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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,226	09/18/2003	Richard M. Ehrlich	PANA-01046USD	6281
23910	7590	08/03/2005	EXAMINER	
FLIESLER MEYER, LLP FOUR EMBARCADERO CENTER SUITE 400 SAN FRANCISCO, CA 94111			FIGUEROA, NATALIA	
			ART UNIT	PAPER NUMBER
			2651	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/665,226	Applicant(s) EHRlich, RICHARD M.	
	Examiner Natalia Figueroa	Art Unit 2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 May 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8, 10-18 and 20-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6, 8, 10, 16, 18 and 20-30 is/are allowed.
- 6) ☒ Claim(s) 1-5, 7, 11-15, and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/31/05, 7/12/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 31 May 2005 (05/31/2005) has been reviewed and is accepted. The terminal disclaimer has been recorded.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 31 May 2005 (05/31/2005) is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.
3. The information disclosure statement (IDS) submitted on 12 July 2005 (07/12/2005) is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-2, 7, 11-12, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bliss (USPN 5,585,975) in view of Kao (USPN 6,816,013).

RE claim 1, Bliss discloses a method for improving servo demodulation robustness in a disk drive system having a read channel including a variable gain amplifier (VGA) (abstract, fig. 1, col. 7, lines 39-40 and col. 10, lines 34-36), the method comprising (a) producing an amplitude

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error signal by comparing a measured servo signal amplitude to a target amplitude (col. 4, lines 58-64 and col. 7, lines 54-55); (b) filtering the amplitude error signal to produce an automatic gain control (AGC) signal useful as feedback to the variable gain amplifier (VGA) of the read channel (col. 7, lines 62-65); and (c) limiting the AGC signal to keep it within a desired range, before providing the AGC signal as an input to the VGA (col. 9, lines 17-21). Bliss fails to explicitly teach that the desired range includes at least one of an upper limit and a lower limit. However, Kao discloses such on (fig. 1 and col. 1, lines 15-16).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as disclosed by Bliss with the above teachings from Kao to include limiting values that would provide controlling of the gain, hence avoiding error operations of the AGC.

RE claim 2, the combination of Bliss and Kao is relied upon for the same reasons of rejection as stated above. Bliss further discloses reading a servo wedge and producing a servo signal therefrom (abstract and col. 1, lines 43-46); and measuring an amplitude of the servo signal (col. 4, lines 52-64 and col. 7, lines 54-55)

RE claim 7, Bliss further discloses that step (a) includes limiting an output path of the digital filter to keep the servo AGC signal within the desired range (col. 9, lines 17-21).

RE claims 11-12 and 17, the combination of Bliss and Kao is relied upon for the same reasons of rejection as stated in the above rejections of claims 1-2 and 7. Claims 11-12 and 17 have limitations similar to those treated in the above rejections of claims 1-2 and 7, and are met by the references as discussed above. Claims 11-12 and 17 however also recites the following

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limitation, a phase locked loop including an oscillator. However, Bliss further discloses such on (col. 3, lines 40-49).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as disclosed by Bliss with the above teachings from Kao to include to limiting values that would provide controlling of the phase, hence avoiding error operations of the PLL.

6. Claims 3-5, and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bliss and Kao and further in view of Cloke et al (USPN 6,487,032), hereinafter Cloke.

RE claim 3, the combination of Bliss and Kao is relied upon for the same reasons of rejection as stated above. Bliss and Kao fail to explicitly teach that the disk drive system includes a plurality of heads, and wherein the desired range is dependent at least in part on which head is being used to read a servo wedge. However, Cloke discloses such on (col. 5, lines 7-8 and 13).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system as disclosed by Bliss with the above teachings from Cloke therefore providing the and adjusting the frequency for each head, hence avoiding errors or loss of data.

RE claim 4, the combination of Bliss, Kao and Cloke is relied upon for the same reasons of rejection as stated above. Cloke further discloses that the disk drive system includes a zone bit recorded disk including a plurality of zones, and wherein the desired range is dependent at least in part on which zone is being read (col. 11, lines 51-55, col. 11, line 63-col. 12, line 10).

RE claim 5, the combination of Bliss, Kao and Cloke is relied upon for the same reasons

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of rejection as stated above. Claim 5 has limitations similar to those treated in the above rejections of claims 3 and 4, and is met by the references as discussed above.

RE claims 13-15, the combination of Bliss, Kao, and Cloke is relied upon for the same reasons of rejection as stated in the above rejections of claims 3-5. Claims 13-15 have limitations similar to those treated in the above rejections of claims 3-5, and are met by the references as discussed above. Claims 13-15 however also recites the following limitation, a phase locked loop. However, Bliss further discloses such on (col. 3, lines 40-49).

Allowable Subject Matter

7. Claims 6, 8, 10, 16, 18, and 20-30 allowed.

8. The following is an examiner's statement of reasons for allowance:

RE claim 6, the prior art of record, and in particular Bliss (USPN 5,585,975) fails to teach or suggest a method comprising (b) filtering the amplitude error signal to produce an automatic gain control (AGC) signal useful as feedback to the variable gain amplifier (VGA) of the read channel; and (c) limiting the AGC signal to keep it within a desired range, before providing the AGC signal as an input to the VGA; wherein step (b) includes (b.1) filtering the amplitude error signal using a digital filter including an integration path; and (b.2) limiting the integration path within the digital filter to thereby prevent integral windup.

Re claim 8, the prior art of record, and in particular Bliss (USPN 5,585,975) fails to teach or suggest a method comprising (c) limiting the AGC signal to keep it within a desired range, before providing the AGC signal as an input to the VGA; wherein step (c) includes (c.1) comparing each servo automatic gain control (AGC) value, of the servo AGC signal, to an upper limit and a lower limit; (c.2) if the servo AGC value is above the upper limit, limiting the servo

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AGC value to the upper limit; and (c.3) if the servo AGC value is below the lower limit, limiting the servo AGC value to the lower limit.

RE claim 10, the prior art of record, and in particular Bliss (USPN 5,585,975) fails to teach or suggest a method comprising (a) comparing a servo automatic gain control (AGC) value to an upper limit and a lower limit; (b) if the servo AGC value is above the upper limit, limiting the servo AGC value to the upper limit; and (c) if the servo AGC value is below the lower limit, limiting the servo AGC value to the lower limit.

RE claim 16, the prior art of record, and in particular Bliss (USPN 5,585,975) fails to teach or suggest a method comprising (b) filtering the phase error signal to produce a servo phase lock loop (PLL) signal useful as feedback to an oscillator; and (c) limiting the PLL signal to keep it within a desired range, before providing the PLL signal as an input to the oscillator; wherein step (b) includes (b.1) filtering the PLL signal using a digital filter including an integration path; and (b.2) limiting the integration path within the digital filter to thereby prevent integral windup.

RE claim 18, the prior art of record, and in particular Bliss (USPN 5,585,975) fails to teach or suggest a method comprising (c) limiting the PLL signal to keep it within a desired range, before providing the PLL signal as an input to the oscillator; wherein step (c) includes (c.1) comparing each servo PLL value, of the servo PLL signal, to an upper limit and a lower limit; (c.2) if the servo PLL value is above the upper limit, limiting the servo PLL value to the upper limit; and (c.3) if the servo PLL value is below the lower limit, limiting the servo PLL value to the lower limit.

RE claim 20, the prior art of record, and in particular Bliss (USPN 5,585,975) fails to

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teach or suggest a method comprising (a) comparing a servo phase lock loop (PLL) value to an upper limit and a lower limit; (b) if the servo PLL value is above the upper limit, limiting the servo PLL value to the upper limit; and (c) if the servo PLL value is below the lower limit, limiting the servo PLL value to the lower limit.

RE claim 21, the prior art of record, and in particular Bliss (USPN 5,585,975) fails to teach or suggest a method comprising (c) storing the servo AGC value in a register; (d) if the servo AGC value stored in the register is outside a desired range, replacing the servo AGC value stored in the register with a value that is within the desired range; and (e) using the servo AGC value stored in the register as, or to predict, a starting AGC value when beginning to read a next servo wedge.

RE claim 26, the prior art of record, and in particular Bliss (USPN 5,585,975) fails to teach or suggest a method comprising (c) storing the servo PLL value in a register; (d) if the servo PLL value stored in the register is outside a desired range, replacing the servo PLL value stored in the register with a value that is within the desired range; and (e) using the servo PLL value stored in the register as, or to predict, a starting servo PLL value when beginning to read a next servo wedge.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments with respect to claims 1-5, 7, 11-15, and 17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Natalia Figueroa whose telephone number is (571) 272-7554. The examiner can normally be reached on Monday - Thursday 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David R. Hudspeth can be reached on (571) 272-7843. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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